In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 to 10. (Canceled)

11. (New) A 4-bit carry look ahead circuit forming a combined propagate signal and a combined generated signal comprising:

a first NAND gate (101) having a first input receiving a propagate signal from a first bit, a second input receiving a propagate signal from the second bit and an output;

a second NAND gate (102) having a first input receiving a propagate signal from the third bit, a second input receiving a propagate signal from the fourth bit and an output;

a NOR gate (103) having a first input connected to said output of said first NAND gate, a second input connected to said output of said second NAND gate and an output forming the combined propagate signal for the four bits;

a first AND-NOR gate (201) having a first AND input receiving a generate signal from the first bit, a second AND input receiving a propagate signal from the second bit, a NOR input receiving a generate signal from the second bit and an output;

a second AND-NOR gate (202) having a first AND input receiving a generate signal from the third bit, a second AND input receiving a propagate signal from the fourth bit, a NOR input receiving a generate signal from the fourth bit and an output; and

a OR-NAND gate (251) having a first OR input connected to said output of said first AND-NOR gate, a second OR input connected to said output of said second NAND gate, a NAND input

connected to said output of said second AND-NOR gate and an output forming the combined generate signal for the four bits.

12. (New) The carry look ahead circuit of claim 11, wherein:
said first and second AND-NOR gates include
a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said first AND input,
a second P-channel transistor having a source-drain path connected between a supply voltage and said first intermediate node and a gate connected to said second AND input,
a third P-channel transistor having a source-drain path connected between said first intermediate node and the output and a gate connected to said NOR input,
a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first AND input,
a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second AND input, and
a third N-channel transistor having a source-drain path connected between said output and ground and a gate connected to said NOR input.

13. (New) The carry look ahead circuit of claim 11, wherein:
said first and second AND-NOR gates include
a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said NOR input,
a second P-channel transistor having a source-drain path connected between a supply voltage and said first

intermediate node and said output and a gate connected to said first AND input,

a third P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said second AND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first AND input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second AND input, and

a third N-channel transistor having a source-drain path connected between said output and ground and a gate connected to said NOR input.

14. (New) The carry look ahead circuit of claim 11, wherein:

said OR-NAND gate includes

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said second OR input,

a second P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said first OR input,

a third P-channel transistor having a source-drain path connected between the supply voltage and said output and a gate connected to said NAND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said OR input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said first OR input, and

a third N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second OR input.

15. (New) The carry look ahead circuit of claim 11, wherein:

said OR-NAND gate includes

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said second OR input,

a second P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said first OR input,

a third P-channel transistor having a source-drain path connected between the supply voltage and said output and a gate connected to said NAND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first OR input,

a second N-channel transistor having a source-drain path connected between said output and said second intermediate node and a gate connected to said second OR input, and

a third N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said NAND input.

16. (New) A 5-bit carry look ahead circuit forming a combined propagate signal and a combined generated signal comprising:

a first NAND gate (104) having a first input receiving a propagate signal from the first bit, a second input receiving a propagate signal from the second bit and an output;

a second NAND gate (105) having a first input receiving a propagate signal from the third bit, a second input receiving a propagate signal from the fourth bit and an output;

a first NOR gate (106) having a first input connected to said output of said first NAND gate, a second input connected to said output of said second NAND gate and an output;

a second NOR gate (107) having a first input connected to said output of said first NOR gate, a second input receiving a propagate signal from the fifth bit and an output;

a first inverter (301) having a input connected to said output of said second NOR gate and an output generating the combined propagate signal for the five bits;

a first AND-NOR gate (203) having a first AND input receiving a generate signal from the first bit, a second AND input receiving a propagate signal from the second bit, a NOR input receiving a generate signal from the second bit and an output;

a second AND-NOR gate (204) having a first AND input receiving a generate signal from the third bit, a second AND input receiving a propagate signal from the fourth bit, a NOR input receiving a generate signal from the fourth bit and an output;

a OR-NAND gate (252) having a first OR input connected to said output of said first AND-NOR gate, a second OR input connected to said output of said second NAND gate, a NAND input connected to said output of said second AND-NOR gate and an output forming the combined generate signal for the four bits;

a third AND-NOR gate (205) having a first AND input connected to said output of said OR-NAND gate, a second AND input receiving a propagate signal from the fifth bit, a NOR input receiving a generate signal from the fifth bit and an output; and

a second inverter (302) having an input connected to said output of said third AND-NOR gate and an output generating the combined generate signal for the five bits.

17. (New) The carry look ahead circuit of claim 16, wherein:
said first, second and third AND-NOR gates include
a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said first AND input,
a second P-channel transistor having a source-drain path connected between a supply voltage and said first intermediate node and a gate connected to said second AND input,
a third P-channel transistor having a source-drain path connected between said first intermediate node and the output and a gate connected to said NOR input,
a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first AND input,
a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second AND input, and
a third N-channel transistor having a source-drain path connected between said output and ground and a gate connected to said NOR input.

18. (New) The carry look ahead circuit of claim 16, wherein:
said first, second and third AND-NOR gates include
a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said NOR input,

a second P-channel transistor having a source-drain path connected between a supply voltage and said first intermediate node and said output and a gate connected to said first AND input,

a third P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said second AND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first AND input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second AND input, and

a third N-channel transistor having a source-drain path connected between said output and ground and a gate connected to said NOR input.

19. (New) The carry look ahead circuit of claim 16, wherein:

said OR-NAND gate includes

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said second OR input,

a second P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said first OR input,

a third P-channel transistor having a source-drain path connected between the supply voltage and said output and a gate connected to said NAND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said OR input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said first OR input, and

a third N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second OR input.

20. (New) The carry look ahead circuit of claim 16, wherein:

said OR-NAND gate includes

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said second OR input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first OR input,

a second P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said first OR input,

a third P-channel transistor having a source-drain path connected between the supply voltage and said output and a gate connected to said NAND input,

a second N-channel transistor having a source-drain path connected between said output and said second intermediate node and a gate connected to said second OR input, and

a third N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said NAND input.

21. (New) A 5-bit carry look ahead circuit forming a combined propagate signal and a combined generated signal comprising:

a first NAND gate (108) having a first input receiving a propagate signal from the first bit, a second input receiving a propagate signal from the second bit and an output;

a second NAND gate (109) having a first input receiving a propagate signal from the third bit, a second input receiving a propagate signal from the fourth bit and an output;

a first inverter (303) having an input connected to said output of said second NAND gate and an output;

a third NAND gate (119) having a first input connected to said output of said first inverter, a second input receiving a propagate signal from the fifth bit and an output;

a NOR gate (111) having a first input connected to said output of said first NAND gate, a second input connected to said output of said third NAND gate and an output generating the combined propagate signal for the five bits;

a first AND-NOR gate (206) having a first AND input receiving a generate signal from the first bit, a second AND input receiving a propagate signal from the second bit, a NOR input receiving a generate signal from the second bit and an output;

a second AND-NOR (207) gate having a first AND input receiving a generate signal from the third bit, a second AND input receiving a propagate signal from the fourth bit, a NOR input receiving a generate signal from the fourth bit and an output;

a second inverter (304) having an input connected to said output of said second AND-NOR gate and an output;

a third AND-NOR gate (208) having a first AND input connected to said output of said second inverter, a second AND input receiving a propagate signal from the fifth bit, a NOR input receiving a generate signal from the fifth bit and an output; and

a OR-NAND gate (253) having a first OR input connected to said output of said first AND-NOR gate, a second OR input connected to said output of said third AND-NOR gate, a NAND input connected to said output of said third AND-NOR gate and an output forming the combined generate signal for the four bits.

22. (New) The carry look ahead circuit of claim 21, wherein:
said first, second and third AND-NOR gates include
a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said first AND input,
a second P-channel transistor having a source-drain path connected between a supply voltage and said first intermediate node and a gate connected to said second AND input,
a third P-channel transistor having a source-drain path connected between said first intermediate node and the output and a gate connected to said NOR input,
a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first AND input,
a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second AND input, and
a third N-channel transistor having a source-drain path connected between said output and ground and a gate connected to said NOR input.

23. (New) The carry look ahead circuit of claim 21, wherein:
said first, second and third AND-NOR gates include

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said NOR input,

a second P-channel transistor having a source-drain path connected between a supply voltage and said first intermediate node and said output and a gate connected to said first AND input,

a third P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said second AND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first AND input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second AND input, and

a third N-channel transistor having a source-drain path connected between said output and ground and a gate connected to said NOR input.

24. (New) The carry look ahead circuit of claim 21, wherein: said OR-NAND gate includes

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said second OR input,

a second P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said first OR input,

a third P-channel transistor having a source-drain path connected between the supply voltage and said output and a gate connected to said NAND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said OR input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said first OR input, and

a third N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second OR input.

25. (New) The carry look ahead circuit of claim 21, wherein: said OR-NAND gate includes

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said second OR input,

a second P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said first OR input,

a third P-channel transistor having a source-drain path connected between the supply voltage and said output and a gate connected to said NAND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first OR input,

a second N-channel transistor having a source-drain path connected between said output and said second intermediate node and a gate connected to said second OR input, and

a third N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said NAND input.

26. (New) A 5-bit carry look ahead circuit forming a combined propagate signal and a combined generated signal comprising:

a first NAND gate (112) having a first input receiving a propagate signal from the second bit, a second input receiving a propagate signal from the third bit and an output;

a second NAND gate (113) having a first input receiving a propagate signal from the fourth bit, a second input receiving a propagate signal from the fifth bit and an output;

a NOR gate (114) having a first input connected to said output of said first NAND gate, a second input connected to said output of said second NAND gate and an output;

a third NAND gate (115) having a first input receiving the propagate signal from the first bit, a second input connected yo said output of said NOR gate and an output;

a first inverter (305) having an input connected to said output of said third NAND gate and an output generating the combined propagate signal for the five bits;

a first AND-NOR gate (209) having a first AND input receiving a propagate signal from the third bit, a second AND input receiving a generate signal from the second bit, a NOR input receiving a generate signal from the third bit and an output;

a second AND-NOR (210) gate having a first AND input receiving a propagate signal from the fifth bit, a second AND input receiving a generate signal from the fourth bit, a NOR input receiving a generate signal from the fifth bit and an output;

a OR-NAND gate (254) having a first OR input connected to said output of said first AND-NOR gate, a second OR input connected to said output of said second NAND gate, a NAND input

connected to said output of said first AND-NOR gate and an output;

a third AND-NOR gate (211) having a first AND input connected to said output of said NOR gate, a second AND input receiving a generate signal from the first bit, a NOR input connected to said output of said OR-NAND gate and an output; and

a second inverter (306) having an input connected to said output of said third AND-NOR gate and an output generation the combined generate signal for the five bits.

27. (New) The carry look ahead circuit of claim 26, wherein:

said first, second and third AND-NOR gates include

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said first AND input,

a second P-channel transistor having a source-drain path connected between a supply voltage and said first intermediate node and a gate connected to said second AND input,

a third P-channel transistor having a source-drain path connected between said first intermediate node and the output and a gate connected to said NOR input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first AND input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second AND input, and

a third N-channel transistor having a source-drain path connected between said output and ground and a gate connected to said NOR input.

28. (New) The carry look ahead circuit of claim 26, wherein: said first, second and third AND-NOR gates include

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said NOR input,

a second P-channel transistor having a source-drain path connected between a supply voltage and said first intermediate node and said output and a gate connected to said first AND input,

a third P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said second AND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first AND input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second AND input, and

a third N-channel transistor having a source-drain path connected between said output and ground and a gate connected to said NOR input.

29. (New) The carry look ahead circuit of claim 26, wherein: said OR-NAND gate includes

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said second OR input,

a second P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said first OR input,

a third P-channel transistor having a source-drain path connected between the supply voltage and said output and a gate connected to said NAND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said OR input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said first OR input, and

a third N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second OR input.

30. (New) The carry look ahead circuit of claim 26, wherein: said OR-NAND gate includes

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said second OR input,

a second P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said first OR input,

a third P-channel transistor having a source-drain path connected between the supply voltage and said output and a gate connected to said NAND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first OR input,

a second N-channel transistor having a source-drain path connected between said output and said second intermediate node and a gate connected to said second OR input, and

a third N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said NAND input.

31. (New) A 5-bit carry look ahead circuit forming a combined propagate signal and a combined generated signal comprising:

a first NAND gate (116) having a first input receiving a propagate signal from the second bit, a second input receiving a propagate signal from the third bit and an output;

a second NAND gate (117) having a first input receiving a propagate signal from the fourth bit, a second input receiving a propagate signal from the fifth bit and an output;

a NOR gate (118) having a first input connected to said output of said first NAND gate, a second input connected to said output of said second NAND gate and an output;

a third NAND gate (119) having a first input receiving the propagate signal from the first bit, a second input connected to said output of said NOR gate and an output;

a first inverter (310) having an input connected to said output of said third NAND gate and an output generating the combined propagate signal for the five bits;

a first AND-NOR gate (212) having a first AND input receiving a propagate signal from the third bit, a second AND input receiving a generate signal from the second bit, a NOR input receiving a generate signal from the third bit and an output;

a second AND-NOR (213) gate having a first AND input receiving a propagate signal from the fifth bit, a second AND input receiving a generate signal from the fourth bit, a NOR input receiving a generate signal from the fifth bit and an output;

a second inverter (307) having an input receiving a generate signal from the first bit and an output;

a OR-NAND gate (255) having a first OR input connected to said output of said first NAND gate, a second OR input connected to said output of said second inverter, a NAND input connected to said output of said first AND-NOR gate and an output;

a third inverter (308) having an input connected to said output of said second NAND gate and an output;

a fourth inverter (309) having an input connected to said output of said second AND-NOR gate and an output;

a third AND-NOR (214) gate having a first AND input connected to said output of said OR-NAND gate, a second AND input connected to said output of said third inverter, a NOR input connected to said output of said fourth inverter and an output; and

a fifth inverter (311) having an input connected to said output of said third AND-NOR gate and an output generating the combined generate signal for the five bits.

32. (New) The carry look ahead circuit of claim 31, wherein:

said first, second and third AND-NOR gates include

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said first AND input,

a second P-channel transistor having a source-drain path connected between a supply voltage and said first intermediate node and a gate connected to said second AND input,

a third P-channel transistor having a source-drain path connected between said first intermediate node and the output and a gate connected to said NOR input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first AND input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second AND input, and

a third N-channel transistor having a source-drain path connected between said output and ground and a gate connected to said NOR input.

33. (New) The carry look ahead circuit of claim 31, wherein: said first, second and third AND-NOR gates include

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said NOR input,

a second P-channel transistor having a source-drain path connected between a supply voltage and said first intermediate node and said output and a gate connected to said first AND input,

a third P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said second AND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first AND input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second AND input, and

a third N-channel transistor having a source-drain path connected between said output and ground and a gate connected to said NOR input.

34. (New) The carry look ahead circuit of claim 31, wherein: said OR-NAND gate includes

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said second OR input,

a second P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said first OR input,

a third P-channel transistor having a source-drain path connected between the supply voltage and said output and a gate connected to said NAND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said OR input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said first OR input, and

a third N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second OR input.

35. (New) The carry look ahead circuit of claim 31, wherein: said OR-NAND gate includes

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said second OR input,

a second P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said first OR input,

a third P-channel transistor having a source-drain path connected between the supply voltage and said output and a gate connected to said NAND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first OR input,

a second N-channel transistor having a source-drain path connected between said output and said second intermediate node and a gate connected to said second OR input, and

a third N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said NAND input.

36. (New) A 6-bit carry look ahead circuit forming a combined propagate signal and a combined generated signal comprising:

a first NAND gate (120) having a first input receiving a propagate signal from the first bit, a second input receiving a propagate signal from the second bit and an output;

a second NAND gate (121) having a first input receiving a propagate signal from the third bit, a second input receiving a propagate signal from the fourth bit and an output;

a third NAND gate (122) having a first input receiving a propagate signal from the fifth bit, a second input receiving a propagate signal from the sixth bit and an output;

a NOR gate (123) having a first input connected to said output of said first NAND gate, a second input connected to said output of said second NAND gate and an output;

a first inverter (315) having an input connected to said output of said third NAND gate and an output;

a fourth NAND gate (124) having a first input connected to said output of said third NOR gate, a second input connected to said output of said first inverter and an output;

a second inverter (316) having an input connected to said output of said fourth NAND gate and an output generating the combined propagate signal for the six bits;

a first AND-NOR gate (215) having a first AND input receiving a generate signal from the first bit, a second AND input receiving a propagate signal from the second bit, a NOR input receiving a generate signal from the second bit and an output;

a second AND-NOR (216) gate having a first AND input receiving a propagate signal from the fourth bit, a second AND input receiving a generate signal from the third bit, a NOR input receiving a generate signal from the fourth bit and an output;

a first OR-NAND gate (256) having a first OR input connected to said output of said first AND-NOR gate, a second OR input connected to said output of said second NAND gate, a NAND input connected to said output of said second AND-NOR gate and an output;

a third inverter (312) having an input receiving a generate signal of the fifth bit and an output;

a fourth inverter (313) having an input connected receiving a propagate signal of the sixth bit and an output;

a fifth inverter (314) having an input receiving a generate signal of the sixth bit and an output;

a second OR-NOR gate (256) gate having a first OR input connected to said output of said third inverter, a second OR input connected to said output of said fourth inverter, a NAND input connected to said output of said fourth inverter and an output; and

a third AND-NOR gate (217) having a first AND input connected to said output of said first OR-NOR gate, a second AND input connected to said output of said second inverter, a NOR input and an output;

a sixth inverter (317) having an input connected to said output of said third AND-NOR gate and an output generating the combined generate signal for the six bits.

37. (New) The carry look ahead circuit of claim 36, wherein:
said first, second and third AND-NOR gates include
a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said first AND input,
a second P-channel transistor having a source-drain path connected between a supply voltage and said first intermediate node and a gate connected to said second AND input,
a third P-channel transistor having a source-drain path connected between said first intermediate node and the output and a gate connected to said NOR input,
a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first AND input,
a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second AND input, and
a third N-channel transistor having a source-drain path connected between said output and ground and a gate connected to said NOR input.

38. (New) The carry look ahead circuit of claim 36, wherein:
said first, second and third AND-NOR gates include
a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said NOR input,

a second P-channel transistor having a source-drain path connected between a supply voltage and said first intermediate node and said output and a gate connected to said first AND input,

a third P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said second AND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first AND input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second AND input, and

a third N-channel transistor having a source-drain path connected between said output and ground and a gate connected to said NOR input.

39. (New) The carry look ahead circuit of claim 36, wherein:

said first and second OR-NAND gates include

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said second OR input,

a second P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said first OR input,

a third P-channel transistor having a source-drain path connected between the supply voltage and said output and a gate connected to said NAND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said OR input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said first OR input, and

a third N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second OR input.

40. (New) The carry look ahead circuit of claim 36, wherein: said first and second OR-NAND gate include

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said second OR input,

a second P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said first OR input,

a third P-channel transistor having a source-drain path connected between the supply voltage and said output and a gate connected to said NAND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first OR input,

a second N-channel transistor having a source-drain path connected between said output and said second intermediate node and a gate connected to said second OR input, and

a third N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said NAND input.

41. (New) A 6-bit carry look ahead circuit forming a combined propagate signal and a combined generated signal comprising:

a first NAND gate (125) having a first input receiving a propagate signal from the first bit, a second input receiving a propagate signal from the second bit and an output;

a second NAND gate (126) having a first input receiving a propagate signal from the third bit, a second input receiving a propagate signal from the fourth bit and an output;

a third NAND gate (127) having a first input receiving a propagate signal from the fifth bit, a second input receiving a propagate signal from the sixth bit and an output;

a first NOR gate (128) having a first input connected to said output of said second NAND gate, a second input connected to said output of said third NAND gate and an output;

a first inverter (319) having an input connected to said output of said first NOR gate and an output;

a second NOR gate (129) having a first input connected to said output of said first NAND gate, a second input connected to said output of said first inverter and an output generating the combined propagate signal for the six bits;

a first AND-NOR gate (218) having a first AND input receiving a propagate signal from the second bit, a second AND input receiving a generate signal from the first bit, a NOR input receiving a generate signal from the second bit and an output;

a second inverter (318) having an input connected to said output of said first AND-NOR gate and an output;

a second AND-NOR (219) gate having a first AND input receiving a propagate signal from the fourth bit, a second AND input receiving a generate signal from the third bit, a NOR input receiving a generate signal from the fourth bit and an output;

a third AND-NOR (220) gate having a first AND input receiving a propagate signal from the sixth bit, a second AND input receiving a generate signal from the fifth bit, a NOR input receiving a generate signal from the sixth bit and an output;

a OR-NAND gate (258) having a first OR input connected to said output of said second AND-NOR gate, a second OR input connected to said output of said third NAND gate, a NAND input connected to said output of said third AND-NOR gate and an output;

a fourth AND-NOR gate (221) having a first AND input connected to said output of said first OR-NOR gate, a second AND input connected to said output of said first NOR gate, a NOR input and an output; and

a third inverter (320) having an input connected to said output of said fourth AND-NOR gate and an output generating the combined generate signal for the six bits.

42. (New) The carry look ahead circuit of claim 41, wherein:

said first, second, third and fourth AND-NOR gates include

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said first AND input,

a second P-channel transistor having a source-drain path connected between a supply voltage and said first intermediate node and a gate connected to said second AND input,

a third P-channel transistor having a source-drain path connected between said first intermediate node and the output and a gate connected to said NOR input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first AND input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second AND input, and

a third N-channel transistor having a source-drain path connected between said output and ground and a gate connected to said NOR input.

43. (New) The carry look ahead circuit of claim 41, wherein: said first, second, third and fourth AND-NOR gates include

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said NOR input,

a second P-channel transistor having a source-drain path connected between a supply voltage and said first intermediate node and said output and a gate connected to said first AND input,

a third P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said second AND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first AND input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second AND input, and

a third N-channel transistor having a source-drain path connected between said output and ground and a gate connected to said NOR input.

44. (New) The carry look ahead circuit of claim 41, wherein: said OR-NAND gate includes

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said second OR input,

a second P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said first OR input,

a third P-channel transistor having a source-drain path connected between the supply voltage and said output and a gate connected to said NAND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said OR input,

a second N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said first OR input, and

a third N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said second OR input.

45. (New) The carry look ahead circuit of claim 41, wherein:

said OR-NAND gate includes

a first P-channel transistor having a source-drain path connected between a supply voltage and an first intermediate node and a gate connected to said second OR input,

a second P-channel transistor having a source-drain path connected between said first intermediate node and said output and a gate connected to said first OR input,

a third P-channel transistor having a source-drain path connected between the supply voltage and said output and a gate connected to said NAND input,

a first N-channel transistor having a source-drain path connected between said output and a second intermediate node and a gate connected to said first OR input,

a second N-channel transistor having a source-drain path connected between said output and said second

intermediate node and a gate connected to said second OR input, and

a third N-channel transistor having a source-drain path connected between said second intermediate node and ground and a gate connected to said NAND input.